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Statistical Information Propagation Across Operators for Dynamic Power Estimation on FPGAs

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Abstract

Performance, cost and energy consumption are the main key features to evaluate any embedded system. Low power system is needed then power optimization process is required. To optimize the power dissipation of an embedded system we have to estimate the power consumption first. This paper presents a new power estimation approach at early design phases which is based on the decomposition of a digital system into basic operators. Each operator has its own model which estimates the switching activity and the power consumption. By interconnecting several operators, statistical information like switching activities and percentage of logic high is then propagated to enable a global power estimation of a given system. The approach consists in simply adding the individual power consumption of each operator. The methodology has been evaluated in a use-case. The preliminary results indicate a promising speed-up of the design process with less than 8.0% of error comparing to the classical power estimation tools.

1. Introduction

Due to the technological trends towards high-level integration, high operating frequencies and low cost, Field Programmable Gate Arrays (FPGAs) constitute one of the best solution for rapid prototyping. FPGAs are programmable logic devices which can implement any digital functions for different fields of application. The major drawback of these devices, compared to their ASICs counterparts, is their relatively high power consumption since they are not optimized for a given application and are far more generic and flexible. It is thus necessary to optimize

the power consumption in the design flow of such systems and estimate power in various design stages. The power estimation techniques in FPGA can be divided into two categories according to the abstraction level of the circuit: low level (physical up to RTL) and high level or system level. At low level, transistors, logic gates and registers are specified and fully described physically, whereas at high level, only a global structure or behavioral view is considered. Generally, this last level lacks from technological details which are crucial to get an accurate information on the dissipated power. Accurate power estimation is achieved at low-level with a significant simulation time that is often prohibitive.

In this paper, a power estimation technique is presented, which consists in a high-level modeling and simulation of systems based on basic operators. Each operator has been carefully modeled using low-level information to benefit from the low level approach and get accurate results. Combining low-level information and high-level modeling leads to significant speed-up of the design process with accurate power estimation.

2 Related works

This section details the existing high-level power estimation techniques. Probabilistic and statistical techniques are two types of techniques used for power estimation. Probabilistic methodology is based on input probability of a signal pattern to estimate the internal transitions in a digital block. Then, probabilities are propagated from the inputs through the circuit to get the output probability used for the next circuit [4, 5]. The main drawback in probabilistic methods is that they do not take into account glitches activities and propagation delays where these factors have significant impact on power estimation. Statis-

tical techniques, as presented in [3], are based on a randomly generated input patterns and consist in monitoring power dissipation through a specific power tool. With this approach, accurate results require a huge number of input patterns to cover different scenarios. A significant simulation time is usually deplored and constitutes a critical limitation for these techniques. In the work of [2], a methodology was proposed, based on real measurements, which allows to model power consumption with architectural and algorithmic parameters. Design reuse is a key advantage of this method. In [1], a power estimation technique at RTL level is proposed. It enables the power estimation of a macro (e.g. adder) or an IP directly from the study of the inputs/outputs statistical properties. Their models deliver an average error ranging from 9% to 15%.

3 Methodology

The total power dissipated in FPGA has two origins: first the static power, second the dynamic power. In this work, we will only focus on dynamic power, since it is the major type of power that can be optimized during the design. The hardware system can be represented by basic operators that exchange data with each other. Each operator may be fully characterized in terms of statistical input/output relationship and power consumption after FPGA implementation. Each component model consists of two sub-models $M1$ and $M2$ that are described in Fig. 1. $M1$ is used to estimate the dynamic power from the sig-

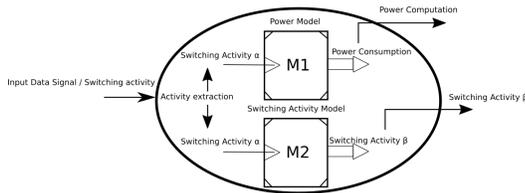


Figure 1. Operator Model

nal activity of the operator’s inputs and from the percentage high parameter. It provides an average of the energy consumed during a period of 1s. The signal activity of the inputs is expressed in terms of millions of transitions per second (Mtr/sec). $M2$ enables to estimate the signal activity of the outputs (as well as the percentage high) and it is useful when designers want to propagate activity among all operators in order to obtain a global power estimation for the entire design. The proposed methodology is composed of 2 steps. Step1: Operator Characterization where each operator is fully implemented on FPGA. After implementation, a low-level power analyzer is used to estimate the average dynamic power that is consumed by the operator. In this step, We obtain $M1$ after timing simulations with randomly generated input metrics i.e. switching activity rate and percentage high. Both (α, p) are the input metrics of the two models while power dissipation and (β, h) are the output metrics for $M1$ and $M2$ respectively. Step2: is the system build and simulation phase

where a system may be built by connecting different operators. The functionality as well as the power models are described in SystemC in order to ease the interoperability between components. A simple example on the methodology can be described here: for a system composed of N operators, the total power consumption can be derived. Let us assume that the switching activity rate is α_i , and that p_i is the % high at the input of op_i . Therefore (β_i, h_i) constitutes the output feature vector of the operator. α_1 and p_1 respectively correspond to the switching activity and percentage high at the input of the op_1 given by the input stimuli. $M_{1,i}$ and $M_{2,i}$ are the two models for the op_i , then by propagating these information to the next operators for power consumption computation a total power can be expressed as in eq. 1.

$$P_{Global} = M_{1,1}(\alpha_1, p_1) + \sum_{i=2}^{N-1} M_{1,i}(\beta_{i-1}, h_{i-1}). \quad (1)$$

4 Results

In this section, a case study is evaluated using a multiplier accumulator (MAC) operator, and a parallel to serial converter. We have chosen these operators as basic operators to build a neural network circuit on FPGA. Each operator is modeled as shown in Fig. 1. A complete model of a neural network is depicted in Fig. 2. Note that $op1$ and $op2$ represent the MAC and P2S respectively. After high

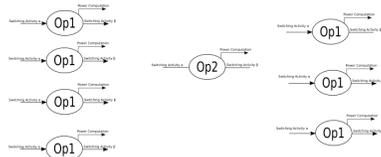


Figure 2. Neural Network Model

level simulation of the neural network model, and after the use of the power analyzer to estimate the power consumption of the implemented neural network on FPGA, a comparison of the results is presented in Table 1. Then, percentage of error is computed using eq. 2 where P_{ref} is the power that results from the real implementation of the neural network, and P_{method} is the total power that has been obtained using our models.

$$\%Error = \frac{|P_{Ref} - P_{Method}|}{P_{Ref}} \times 100 \quad (2)$$

Reference_Power (mW)	Methodology_Power (mW)	% Error
239.0	221.0	7.5

Table 1. Model Accuracy vs RT Level

5 Conclusion and future work

In this paper, we have proposed a new approach for the dynamic power estimation on FPGA at system level. It is achieved by the decomposition of a digital system into basic operators. By summing up the estimated power computed by each operator, we are able to obtain a global power estimation. The presented method allows designers to perform early power estimation and efficient power reduction. We have shown that our method provides good results, since the error is less than 8%. In addition to the good accuracy, a speed-up of the design process is noted. As future work, a hardware validation based on real power measurement on FPGA board to model the power consumption of different operators. It is also foreseen to develop and integrate the models with different platforms to facilitate the power estimation at high level of abstraction.

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